

WHAT IS CLAIMED IS:

- 1 1. A power device, comprising:
2 a semiconductor substrate of first conductivity having an upper surface and a
3 lower surface;
4 an isolation diffusion region of second conductivity provided at a periphery of
5 the substrate and extending from the upper surface to the lower surface of the substrate, the
6 isolation diffusion region having a first surface corresponding to the upper surface of the
7 substrate and a second surface corresponding to the lower surface;
8 a peripheral junction region of second conductivity formed at least partly
9 within the isolation diffusion region and formed proximate the first surface of the isolation
10 diffusion region; and
11 first and second terminals.
- 1 2. The device of claim 1, wherein the peripheral junction region is a P+
2 region and the isolation diffusion region is a P region.
- 1 3. The device of claim 1, wherein the peripheral junction region is
2 provided to compensate the surface depletion of the isolation diffusion region.
- 1 4. The device of claim 1, wherein the peripheral junction region has a
2 portion that extends outward from an edge of the isolation diffusion region.
- 1 5. The device of claim 1, further comprising:
2 a reverse blocking guard ring proximate the isolation diffusion region to
3 increase a reverse blocking voltage of the device.
- 1 6. The device of claim 1, wherein the peripheral junction region has a
2 portion that extends outward from an edge of the isolation diffusion region, the device further
3 comprising:
4 a reverse blocking guard ring of second conductivity proximate the isolation
5 diffusion region to increase a reverse blocking voltage of the device;
6 a channel stopper of first conductivity;
7 a first main junction region coupled to the first terminal, the first main junction
8 provided proximate the upper surface of the substrate;

9 a forward blocking guard ring of second conductivity provided between the
10 channel stopper and the first main junction.

1 7. The device of claim 6, further comprising:
2 an oxide layer and a polymid layer provided overlying the upper surface of the
3 substrate to passivate the device.

1 8. The device of claim 7, wherein the oxide layer has fixed charge of
2 about 10^{11} to 2×10^{11} and formed using a wafer having a diameter of 6 inches or greater.

1 9. The device of claim 6, further comprising:
2 a second main junction region coupled to the second terminal and provided
3 proximate the lower surface of the substrate,
4 wherein the device is a thyristor, diode, insulated gate bipolar device, or the
5 like.

1 10. The device of claim 1, further comprising:
2 a first shallow junction region of second conductivity overlying the peripheral
3 junction region, the first shallow junction region including an outward extension that extends
4 outside of the isolation diffusion region.

1 11. The device of claim 10, wherein the first shallow junction is a P region
2 has a depth of no more than 15 microns, wherein the first peripheral junction region has a
3 depth of 30 microns or greater.

1 12. The device of claim 10, further comprising:
2 a reverse blocking shallow junction guard ring of second conductivity
3 provided proximate the isolation diffusion region.

1 13. The device of claim 12, further comprising:
2 a channel stopper of first conductivity;
3 a first main junction region coupled to the first terminal, the first main junction
4 provided proximate the upper surface of the substrate;
5 a forward blocking shallow junction guard ring of second conductivity
6 provided between the channel stopper and the first main junction.

1 14. The device of claim 13, wherein the device including a plurality of the
2 reverse blocking shallow junction guard rings and a plurality of forward blocking shallow
3 junction guard rings, the forward and reverse blocking shallow junction guard rings not
4 extending beyond a depth of 15 microns and being P regions.

1 15. The device of claim 13, further comprising:
2 a second shallow junction region of second conductivity overlying the first
3 main junction and including an outward extension that extends outside of the first main
4 junction.

1 16. The device of claim 15, wherein the first and second shallow junctions
2 and forward and reverse blocking shallow junction guard rings have substantially the same
3 concentration level and depth.

1 17. The device of claim 10, further comprising:
2 a plurality of reverse blocking shallow junction guard rings provided
3 proximate the upper surface of the substrate and the isolation diffusion region.

1 18. The device of claim 10, further comprising:
2 an oxide layer and a polymid layer provided overlying the upper surface of the
3 substrate to passivate the device.

1 19. The device of claim 10, wherein the oxide layer has fixed charge of
2 about 10^{11} to 2×10^{11} and formed using a wafer having a diameter of 6 inches or greater.

1 20. The device of claim 10, further including a passivation layer overlying
2 the upper surface of the substrate, wherein the passivation layer includes oxide, polymid,
3 silicon nitride, diamond-like-carbon, or a combination thereof to withstand high surface
4 electric field and to reduce migration of ions from an environment of the device.

1 21. A power device, comprising:
2 a semiconductor substrate of first conductivity having an upper surface and a
3 lower surface;
4 an isolation diffusion region of second conductivity provided at a periphery of
5 the substrate and extending from the upper surface to the lower surface of the substrate, the

isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface;
a peripheral junction region of second conductivity formed entirely within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, the peripheral junction region having a first depth;
a first shallow junction region of second conductivity overlying the peripheral junction region, the first shallow junction region including an outward extension that extends outside of the isolation diffusion region, the first shallow junction region having a second depth that is less than the first depth;
a first main junction region proximate the upper surface; and
first and second terminals.

22. The device of claim 10, wherein the first shallow junction is a P region, wherein the first depth is no more than 15 microns and the second depth is 35 microns or greater.

23. The device of claim 21, further comprising:
a channel stopper of first conductivity;
a second main junction region proximate the lower surface of the substrate;
and
a plurality of shallow junction guard ring of second conductivity.

24. The device of claim 23, further comprising:
an oxide layer overlying the upper surface of the substrate and having fixed charge of no more than about 2×10^{11} .

25. A power device, comprising:
a semiconductor substrate of first conductivity having an upper surface and a lower surface;
an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate;
a peripheral junction region of second conductivity formed entirely within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, the peripheral junction region having a first depth;

9 a first shallow junction region of second conductivity overlying the peripheral
10 junction region, the first shallow junction region including an outward extension that extends
11 outside of the isolation diffusion region, the first shallow junction region having a second
12 depth that is less than the first depth;
13 a plurality of shallow junction guard rings of second conductivity provided
14 proximate the upper surface of the substrate, the shallow junction guard rings having a third
15 depth that is less than the first depth;
16 a main junction region proximate the upper surface;
17 a second shallow junction region of second conductivity overlying the main
18 junction region, the second shallow junction region including an outward extension that
19 extends outside of the main junction region, the second shallow junction region having a
20 fourth depth that is less than the first depth; and
21 first and second terminals.